CLAIMS

1-18. (canceled)

19. (previously presented) A circuit for deriving a third order signal from an input signal, the circuit comprising:

input circuitry for providing the input signal along first, second and third paths,

a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal, and

a generator for creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

20. (previously presented) A circuit as claimed in claim 19, for deriving a fifth order signal from the input signal, the generator comprising circuitry for providing the second order signal along a second squared signal path, and a third combiner for combining the second order signal from the second squared signal path with the third order signal to produce the fifth order signal.

21. (previously presented) A circuit as claimed in claim 19, for deriving a fifth order signal from the input signal, wherein:

the input circuitry provides the input signal along fourth and fifth paths, and

the generator comprises:

a third combiner for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and

a fourth combiner for combining the input signal from the fifth path with the fourth order signal to produce the fifth order signal.

22. (previously presented) A circuit as claimed in claim 19, wherein the input signal is a radio frequency signal.

23. (previously presented) A circuit as claimed in claim 19, further comprising an injector for injecting a direct current signal into at least one of the signal paths.

24. (previously presented) A circuit as claimed in claim 23, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal.

25. (previously presented) A circuit as claimed in claim 24, further comprising an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

26. (previously presented) A circuit as claimed in claim 25, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

27. (previously presented) A circuit as claimed in claim 19, further comprising an injector for injecting a direct current signal into a second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in a fifth order signal.

28. (previously presented) A circuit as claimed in claim 27, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

29. (previously presented) A circuit as claimed in claim 19, wherein the combiners are selected from mixers and multipliers.

30. (previously presented) A circuit as claimed in claim 19, wherein the input circuitry comprises at least one splitter for providing the input signal along the signal paths.

31. (previously presented) A circuit as claimed in claim 19, wherein the input circuitry comprises at least one directional coupler for providing the input signal along the signal paths.

32. (previously presented) A polynomial predistorter including a circuit for deriving a third order predistortion signal from an input signal, the circuit comprising:
input circuitry for providing the input signal along first, second and third paths,
a first combiner for combining the input signal from the first and the second paths to produce a second order signal on a squared signal path,
a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,
a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal, and
a generator for creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

33. (previously presented) A method of deriving a third order predistortion signal from an input signal, the method comprising:
providing the input signal along first, second and third paths,
combining the input signal from the first and second paths to produce a second order signal on a squared signal path,
low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,
combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal, and
creating at least one further, different, odd-order signal, each said further, different, odd-order signal being created by combining the input signal with itself.

34-36. (canceled)

37. (previously presented) A circuit for deriving a third order signal from an input signal, the circuit comprising:
input circuitry for providing the input signal along first, second and third paths,
a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal;

an injector for injecting a direct current signal into at least one of the signal paths, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal, and

an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

38. (previously presented) A circuit as claimed in claim 37, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

39. (currently amended) A circuit for deriving a third order signal from an input signal, the circuit comprising:

input circuitry for providing the input signal along first, second and third paths,

a first combiner for combining the input signal from the first and second paths to produce a second order signal on a squared signal path,

a filter for low-pass filtering the second order signal to remove components at a frequency of the input signal and harmonics thereof,

a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce the third order signal, and

an injector for injecting [the] a direct current signal into [the] a second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in [the] a fifth order signal.

40. (previously presented) A circuit as claimed in claim 39, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

41. (currently amended) A predistorter for linearizing an amplifier, the predistorter comprising a first set of circuitry adapted to generate a first high-order signal based on an input signal, wherein:

the first high-order signal is used to generate a predistorted input signal for application to the amplifier;

the first set of circuitry is adapted to inject a first DC signal during the generation of the first high-order signal to reduce lower-order tone energy in the first high-order signal; and

the order of the first high-order signal is greater than or equal to ~~five~~ three.

42. (currently amended) The predistorter of claim 41, further comprising:

a second set of circuitry adapted to generate a second high-order signal based on the input signal, wherein:

the first and second high-order signals are used to generate the predistorted input signal; [and]

the order of the second high-order signal is greater than or equal to three and different from the order of the first high-order signal;

the first and second high-order signals are odd-order signals;

the second high-order signal is a third-order signal; and
the second set of circuitry comprises:
a first combiner adapted to combine first and second versions of the input signal to generate a second-order signal;
a second combiner adapted to combine a third version of the input signal with the second-order signal to generate the third-order signal.

43-53. (canceled)

54. (currently amended) The predistorter of claim [48] 42, wherein:
the first high-order signal is a fifth-order signal; and
the first set of circuitry comprises a third combiner adapted to combine a version of the second-order signal with a version of the third-order signal to generate the fifth-order signal.

55-61. (canceled)

62. (new) The predistorter of claim 41, wherein:
the first high-order signal is a third-order signal;
the first set of circuitry (Fig. 2) comprises:
a first combiner (410) adapted to combine first and second versions of the input signal to generate a second-order signal; and
a second combiner (425) adapted to combine a third version of the input signal with the second-order signal to generate the third-order signal; and
the predistorter further comprises a controller (445) adapted to inject the first DC signal during the generation of the third-order signal.

63. (new) The predistorter of claim 62, wherein the controller is adapted to inject the first DC signal into the second-order signal (435) between the first and second combiners.

64. (new) The predistorter of claim 62, wherein the controller is adapted to adaptively generate the first DC signal based on the input signal and the third-order signal.

65. (new) The predistorter of claim 64, wherein the controller (Fig. 3) comprises:
a mixer (455) adapted to combine a version of the input signal and a version of the third-order signal; and
an integrator (460) adapted to generate the first DC signal by integrating the output from the mixer.

66. (new) The predistorter of claim 64, wherein the controller (Fig. 4) comprises:
a third combiner (480) adapted to combine the third-order signal and a first oscillator signal;
a high-pass filter (485) adapted to filter the output from the third combiner;
a fourth combiner (490) adapted to combine the input signal and the output from the high-pass filter;
a fifth combiner (500) adapted to combine the output from the fourth combiner and a second oscillator signal; and
an integrator (505) adapted to generate the first DC signal by integrating the output from the fifth combiner.

67. (new) The predistorter of claim 66, wherein:
the third and fourth combiners and the high-pass filter are implemented in an analog domain; and

the fifth combiner and the integrator are implemented in a digital domain.

68. (new) The predistorter of claim 62, further comprising a second set of circuitry (Fig. 5, 6) adapted to generate a second high-order signal based on the input signal, wherein:
the first and second high-order signals are used to generate the predistorted input signal;
the controller (Fig. 7-9) is adapted to inject a second DC signal during the generation of the second high-order signal to reduce lower-order tone energy in the second high-order signal; and
the order of the second high-order signal is greater than or equal to five and different from the order of the first high-order signal.

69. (new) The predistorter of claim 68, wherein:
the second high-order signal is a fifth-order signal; and
the second set of circuitry (Fig. 5) comprises a third combiner (545) adapted to combine a version of the second-order signal with a version of the third-order signal to generate the fifth-order signal.

70. (new) The predistorter of claim 69, wherein the controller (Fig. 7) is adapted to inject the second DC signal into the version of the second-order signal between the first and third combiners.

71. (new) The predistorter of claim 69, wherein the controller (Fig. 7) is adapted to adaptively generate the second DC signal based on the third-order signal and the fifth-order signal.

72. (new) The predistorter of claim 71, wherein the controller (Figs. 8, 9) comprises:
a fourth combiner adapted to combine a version of the fifth-order signal and a first oscillator signal;
a high-pass filter adapted to filter the output from the fourth combiner;
a fifth combiner adapted to combine a version of the third-order signal and the output from the high-pass filter;
a sixth combiner adapted to combine the output from the fifth combiner and a second oscillator signal; and
an integrator adapted to generate the second DC signal by integrating the output from the sixth combiner.

73. (new) The predistorter of claim 72, wherein:
the fourth and fifth combiners and the high-pass filter are implemented in an analog domain; and
the sixth combiner and the integrator are implemented in a digital domain.

74. (new) The predistorter of claim 68, wherein:
the second high-order signal is a fifth-order signal; and
the second set of circuitry (Fig. 6) comprises:
a third combiner (575) adapted to combine a fourth version of the input signal with the third-order signal to generate a fourth-order signal; and
a fourth combiner (580) adapted to combine a fifth version of the input signal with the fourth-order signal to generate the fifth-order signal.

75. (new) The predistorter of claim 74, wherein the controller is adapted to inject the second DC signal into the fourth version of the input signal before the third combiner.

76. (new) The predistorter of claim 75, wherein the controller is adapted to inject a third DC signal into the fifth version of the input signal before the fourth combiner.

77. (new) The predistorter of claim 68, further comprising a third set of circuitry (Fig. 10) adapted to generate a third high-order signal based on the input signal, wherein:

the first, second, and third high-order signals are used to generate the predistorted input signal; and

the order of the third high-order signal is greater than or equal to seven and different from the orders of the first and second high-order signals.

78. (new) The predistorter of claim 77, wherein:

the third high-order signal is a seventh-order signal; and

the third set of circuitry comprises a fourth combiner adapted to combine a version of the second-order signal with a version of the fifth-order signal to generate the seventh-order signal.

79. (new) The predistorter of claim 68, wherein the predistorter (Fig. 1) further comprises:

a variable phase-shift block (235) and a variable attenuator block (240) adapted to apply a selected phase shift and a selected attenuation level, respectively, to each of the first and second high-order signals;

a first summation node (245) adapted to combine the phase-shifted, attenuated, first and second high-order signals to form a polynomial predistortion signal;

an amplifier (250) adapted to amplify the polynomial predistortion signal; and

a second summation node (220) adapted to combine the amplified, polynomial predistortion signal with the input signal to generate the predistorted input signal.